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EXAMINER	
IWASHKO, LEV	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,982	TRAN ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The seven replacement drawings have been acknowledged and are deemed in compliance.

2. No claims have been amended or cancelled.

3. Claims 1-36 stand rejected.

Claim Rejections - 35 USC § 102

4. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-8, 10-15, 17-20, 22, 24-31, and 33-36 are rejected under U.S.C. 102(e) as being anticipated by Matsuzaki et al. (US PGPub 2003/0135699 A1).

Claim 1. A data processor core comprising:

- a clock signal input operable to receive a processor clock signal;
  (Figure 1 – Shows clock input signals)

- a memory access interface portion operable to perform data transfer operations between an external data source and at least one memory associated with said data processor core in response to receipt of said processor clock signal; *(Section 0697, lines 1-17 – State the following: "In the late-write operation, data and an address provided from the exterior of the device are temporarily stored in buffers, and the data stored in the buffers are written in the memory cells at the next write operation. Namely, the data and address supplied from the exterior of the device at a given write operation are temporarily stored in buffers, and the data stored in the buffers are written during the next write operation in the memory cells specified by the address stored in the buffers. Data and an address newly provided at the second write operation are temporarily stored in the buffers in the like manner, thereby preparing for the following write operation. In this manner, the actual writing of data in memory cells is delayed from a given write operation to the next write operation, thereby making it possible to access the memory core at the start of the next write operation cycle. This provides an interface that is compatible to the SRAM interface")*
- a data processing portion operable to perform further data processing operations in response to receipt of said processor clock signal; *(Section 0141, lines 1-4 – State the following: "FIG. 121 shows operations performed when the cycles of the clock signals CLKA and CLKB are the same, and the phase of the clock signal CLKA is ahead of the phase of the clock signal CLKB by more than half a cycle")*
- at least one further input operable to receive a memory access enable signal; *(Section 0553, lines 6-11 – State the following: "The mode register 5012b, the clock buffer 5024b, the command latch 5026b, the data latch 5028b, the row address buffer 5031b, and the column address latch 5032b corresponding to the input/output port PORT-B*

operate when an enable signal /ENB supplied from the arbitration circuit 5034 is activated")

- at least one read/write port operable to receive and send data via a bus to said at least one memory associated with said data processor core; *(Section 0008,lines 1-7 – State the following: "In a multi-port memory having two ports, for example, one SRAM memory cell is provided with two sets of word lines and bit line pairs. One of the ports performs a read/write operation by using one set of a word line and a bit line pair, and the other one of the ports performs a read/write operation by using the other set of a word line and a bit line pair")*
- wherein said memory access interface portion is operable to receive said processor clock signal when said memory access enable signal has a predetermined value and not to receive said processor clock signal when said memory access enable signal does not have said predetermined value; *(Section 0554, lines 1-4 – State the following: "Namely, at the time of activation of the enable signal /ENA, the clock buffer 5024a supplies the clock signal CLKA to a clock terminal CLK of the memory core 5040." Section 0582, lines 9-14 – State the following: "The enable signal/ENA is deactivated in response to the completion of the read operation (FIG. 120-(j)). Here, the precharge operation charges bit lines for transferring data to and from memory cells to a predetermined potential, and deactivates circuitry relevant to row address operations")*
- and said data processing portion is operable to receive said processor clock signal when a data processing enable signal has a further predetermined value and not to receive said processor clock signal when said data processing enable signal does not have said further predetermined value. *(Figure 1 – Demonstrates the above limitation)*

Claim 2. A data processor core according to claim 1, said data processor core further comprising data processing enable logic operable to generate said

data processing enable signal. *(Section 0717, lines 1-10 – State the following: "In the Busy logic circuit 6071 corresponding to the left-hand-side port L-port, the OR circuit 6083 put together a plurality of Busy_int signals supplied from the timing generator units 6051 corresponding to the respective banks, thereby generating a single Busy signal. When the chip-enable signal/CE.sub.L input into the left-hand-side port L-port is asserted (LOW), the Busy signal is output from the NAND circuit 6081 as a negative-logic signal/BuSY.sub.L. The same is applied in the case of the Busy logic circuit 6072 corresponding to the right-hand-side port R-port")*

Claim 3. A data processor core according to claim 2, wherein said data processing enable signal is operable to generate said data processing enable signal in response to detection of a state of said processor clock and a state of said bus in data communication with said read/write port. *(Section 0256, lines 1-9 – State the following: "Differences from the first embodiment shown in FIG. 4 includes the fact that an A port 11A and a B port 12A are provided with BUSY signal I/O units 36 and 46, respectively, and the fact that an address comparator 26 is provided to compare an address of the A port with an address of the B port. If the address comparator 26 detects an address match and thus generates a match signal, an arbiter 15A will switch operation modes of a DRAM core so as to initiate a continuation mode")*

Claim 4. A data processor core according to claim 1, comprising a second further input, said second further input being operable to receive said data processing enable signal. *(Section 0553, lines 1-11 – State the following: "The mode register 5012a, the clock buffer 5024a, the command latch 5026a, the data latch 5028a, the row address buffer 5031a, and the column address latch 5032a corresponding to the input/output port PORT-A operate when an enable signal /ENA supplied from the arbitration circuit 5034 is activated. The mode register 5012b, the clock*

buffer 5024b, the command latch 5026b, the data latch 5028b, the row address buffer 5031b, and the column address latch 5032b corresponding to the input/output port PORT-B operate when an enable signal /ENB supplied from the arbitration circuit 5034 is activated")

Claim 5. A data processor core according to claim 1, wherein said predetermined value and said further predetermined value are the same. *(Section 0560, lines 1-34 – State the following: "The address comparison circuit 5042 includes two address matching circuits 5042a and an address comparator 5042b, which detects an order of address arrivals. The address matching circuits 5042a includes a plurality of EOR circuits 5042c, each of which compares corresponding bits of the row address signals RA between the address signal ADDA and the address signal ADDB, and further includes a plurality of nMOS transistors 5042d which correspond to the respective EOR circuit 5042c. The nMOS transistors 5042d each have the gate thereof connected to the output of a corresponding EOR circuit 5042c, the source thereof grounded, and the drain thereof connected with each other. Each EOR circuit 5042c outputs a low level signal when bit values of the row address signals RA match each other between the input/output ports PORT-A and PORT-B, and outputs a high level signal when the bit values of the row address signals RA do not match. The nMOS transistors 5042d are turned off in response to the low level signal from the EOR circuits 5042c, and turns on in response to the high level signal. Namely, match signals /COTN1 and /COIN2 output from the address matching circuits 5042a become floating when all the bits of the row address signals RA match between corresponding bits, and become a low level signal when at least one bit of the row address signals differs between corresponding bits. The two address matching circuits 5042a are arranged at the respective upper end and lower end of the memory block MB shown in FIG. 111 (i.e., arranged close to the input/output circuits 5010). Arrangement of the address matching circuits 5042a close to the I/O circuits 5010 makes it*

possible to shorten the propagation delay of the address signals ADDA and ADDB all the way to the address matching circuits 5042a. Consequently, the address signals ADDA and ADDB can be compared at an early timing, thereby attaining a high-speed operation")

Claim 6. A data processor core according to claim 1, wherein said memory access interface is operable to transfer data to or from said at least one memory via said read/write port and said bus. *(Section 0449, lines 1-11 – State the following: "Multi-port memories, which are semiconductor memory devices equipped with a plurality of ports, can be classified into various types. When the term "multi-port memory" is used hereinafter, it refers to a memory that is provided with a plurality of ports, and that allows access to be independently made from any one of the ports to a common memory array. Such a memory may have an A port and a B port, and allows a read/write operation to be conducted with respect to the common memory array independently from a CPU linked to the A port and from a CPU linked to the B port." Section 0465, lines 1-6 – State the following: "A multi-port memory 4010 of FIG. 101 includes an A port 4011, a B port 4012, a self-refresh circuit 4013, memory blocks 4014-1 through 4014-n, an arbiter 4015, a refresh address counter 4016, an address change circuit 4017, an address change circuit 4018, an address comparator 4019, a bus A 4020-1, and a bus B 4020-2")*

Claim 7. A data processor core according to claim 1, wherein said external data source comprises a further memory associated with said processor core. *(Abstract, lines 1-5 – State the following: "A semiconductor memory device includes a plurality of N external ports, each of which receives commands, and an internal circuit which performs at least N access operations during a minimum interval of the commands that are input into one of the external ports")*

Claim 8. A data processor core according to claim 1, wherein said external data source comprises a further memory, said memory access interface being

operable to transfer data to and from said further memory via a direct memory access controller. *(Section 0670, lines 1-12 – State the following: "When the same row address signals RA are supplied to the input/output ports PORT-A and PORT-B, a read operation is performed only in response to one of the ports. Because of this, power consumption during the operation can be reduced compared with a case in which respective read operations are performed with respect to both ports. Use of the page buffers 5050a and 5050b eliminates a need for the controller controlling the multi-port memory memory M to detect a busy state of the multi-port memory M even when a page operation is performed. Consequently, the control (in terms of hardware and software) of the controller or the like becomes easier")*

Claim 10. A data processor core according to claim 1, wherein said memory access enable signal comprises a clock signal having a different frequency to said processor clock signal and periodically, at said different frequency, going from a first state having said predetermined value to a second state not having said predetermined value, said memory interface being operable to receive said processor clock in response to said memory enable signal being in said first state and not to receive said processor clock in response to said memory enable clock signal being in said second state. *(Sections 0594-0596 – State the following: "Since the input/output ports PORT-A and PORT-B have the respective clock terminals CLKA and CLKB, the frequency of the clock signals CLKA and CLKB can be set separately for each one of the input/output ports PORT-A and PORT-B. That is, a plurality of controllers operating on different operation frequencies can be connected to the multi-port memory M. Further, the first one to arrive between the two addresses is decided by using the row address signals RA that are settled before the relevant rising edges of the clock signals CLKA and CLKB. Namely, the first one to arrive is identified by utilizing the setup time tS of address signals. Because of this, an input/output port that*

will be given priority can be identified before the memory core 5040 starts operation thereof, thereby achieving high-speed memory operation. Further, since the first one to arrive is determined based on a rising edge of the clock signal CLKA (or CLKB) having an earlier phase, the memory operation speed can be further enhanced. In the arbitration circuit 5034, the address comparison circuit 5042 compares the row address signals RA, and the arbitration control circuit 5044 checks an address match in synchronization with the clock signals CLKA and CLKB that are used to acquire the active commands ACT. Since the row address signals RA are always compared with each other at a predetermined timing (i.e., at the edge of a clock signal), it is possible to prevent a malfunction of the memory core 5040 caused by address signals irrelevant to memory operations")

Claim 11. A data processor core according to claim 1, further comprising at least one logic gate operable to combine said processor clock signal received at said processor clock signal input with said processor clock enable signal, said at least one logic gate being operable to output said processor clock signal when said processor enable signal has said further predetermined value and not to output said processor clock signal when said processor enable signal does not have said further predetermined value, said data processing portion receiving said output of said at least one logic gate such that said data processing operations performed by said data processing portion are clocked by said output of said at least one logic gate. *(Section 0184, lines 1-7 – State the following: "A multi-port memory 10 of FIG. 4 includes an A port 11, a B port 12, a self-refresh circuit 13, a DRAM core 14, an arbiter 15, a refresh-command register 16, a command register A 17, a command register B 18, a refresh-address register 19, an address register A 20, an address register B 21, a write-data register A 22, a write-data register B 23, a transfer gate A 24, and a transfer gate B 25")*

Claim 12. A data processor core according to claim 1, further comprising at least one logic gate operable to combine said processor clock signal received at said processor clock signal input with said memory access enable signal received at said at least one further input, said at least one logic gate being operable to output said processor clock signal when said memory access enable signal has said predetermined value and not to output said processor clock signal when said memory access enable signal does not have said predetermined value, said memory access interface portion receiving said output of said at least one logic gate such that said data transfer operations performed by said memory access interface are clocked by said output of said at least one logic gate. *(Section 0184, lines 1-7 – State the following: "A multi-port memory 10 of FIG. 4 includes an A port 11, a B port 12, a self-refresh circuit 13, a DRAM core 14, an arbiter 15, a refresh-command register 16, a command register A 17, a command register B 18, a refresh-address register 19, an address register A 20, an address register B 21, a write-data register A 22, a write-data register B 23, a transfer gate A 24, and a transfer gate B 25")*

Claim 13. A data processor according to claim 1, said core further comprising:

- arbitration logic associated with said read/write port; *(Section 0707, lines 1-12 – State the following: "The R/W holding circuit 6053 responds to a row activation signal by storing therein a Read/Write activation signal supplied through the arbitration logic 6031 from the command buffer 6011 or 6021. The Read/Write activation signal is activated when a Read operation or a Write operation is requested by command signals entered from the exterior of the device. The R/W holding circuit 6053 stores therein an access state (i.e., indicative of a write state or a read state) in response to the Read/Write activation signal. The access state stored in the R/W holding circuit 6053 is supplied to the timing generation circuit 6055 as a signal R/W indicative of an access state")*

- wherein said arbitration logic is operable to route a data access request requesting access of data in one portion of said at least one memory received from said memory access interface to one of said at least two buses providing access to said one portion of said at least one memory and to route a further data access request requesting access of data in a further portion of said at least one memory received from said data processing portion to a further one of said at least two buses providing access to said further portion of said at least one memory, said routing of said data access requests being performed during the same clock cycle. *(Sections 0696-0706 – State the following: "The data input output buffer 6013 or 6023 also receives data to be written from the exterior of the device. The data are written in the memory cells selected by a column line among memory cells corresponding to the selected word after traveling through the write amplifier of the data-bus-amplifier-&-write-amplifier unit 6036, the data bus, sense amplifiers, and bit lines. Selection of one of the port L-port and the port R-port at the time of write operation is made by the switch 6037. Further, the data hold buffers 6014 and 6024 are provided for the port L-port and the port R-port, respectively, for the purpose of performing a late-write operation. In the late-write operation, data and an address provided from the exterior of the device are temporarily stored in buffers, and the data stored in the buffers are written in the memory cells at the next write operation. Namely, the data and address supplied from the exterior of the device at a given write operation are temporarily stored in buffers, and the data stored in the buffers are written during the next write operation in the memory cells specified by the address stored in the buffers. Data and an address newly provided at the second write operation are temporarily stored in the buffers in the like manner, thereby preparing for the following write operation. In this manner, the actual writing of data in memory*

cells is delayed from a given write operation to the next write operation, thereby making it possible to access the memory core at the start of the next write operation cycle. This provides an interface that is compatible to the SRAM interface. The refresh timing generation circuit 6040 includes an oscillator 6041 and a divider 6042. The oscillator 6041 generates pulses by oscillation. The generated pulses are subjected to frequency division by the divider 6042, thereby generating a refresh activation signal at constant refresh intervals. The internal address-generation circuit 6039 responds to a refresh activation signal by generating addresses at which refresh operations are to be performed, and supplies these addresses to the address decoder 6015. The refresh activation signal is also supplied to the timing generator 6032. The timing generator 6032 responds to the refresh activation signal by generating timing pulses for performing refresh operations at proper timing, and supplies the timing pulses to the column decoder 6033, the word decoder 6035, etc. In this manner, a refresh command is automatically generated inside the dual-port semiconductor-memory device 6010, thereby making it possible to perform refresh operations at constant intervals with respect to the cell array 6034. Moreover, the dual-port semiconductor memory device 6010 according to the present invention is configured to supply a Busy signal to the exterior of the device if accesses to the same bank are simultaneously made through the port L-port and the port R-port. FIG. 141 is a block diagram showing the configuration of the timing generator 6032 in relation to the generation of Busy signals. As shown in FIG. 141, the timing generator 6032 includes a plurality of timing generator units 6051 provided separately for respective banks #0 through #n. A bank activation signal generated based on an address input into the port L-port or the port R-port is supplied from the address decoder 6015 or 6025 to one of the timing generator unit

6051 corresponding to the specified bank. If the core circuit is already in the activated state by the timing generator unit 6051 when a bank activation signal arrives, the timing generator unit 51 will generate a Busy_int.sub.L signal or a Busy_int.sub.R signal. The generated Busy_int.sub.L signal or Busy_int.sub.R signal is supplied to the arbitration logic 6031, and is then output to the exterior of the device through the arbitration logic 6031. The timing generator unit 6051 retains the input address, and activates the core circuit immediately after the current operation of the core circuit comes to an end. If a bank activation signal is also supplied from the other port, the input address corresponding to this signal is also retained. In order to first select an address that was retained earlier than the other, the provision of FIFO 6052 or the like is made. When a bank activation signal is supplied to the timing generator unit 6051, the corresponding bank may not be in an activated state. In such a case, the core operation will be started immediately. FIG. 142 is a block diagram showing the detailed configuration of the timing generator unit 6051. The timing generator unit 6051 of FIG. 142 includes a FIFO circuit 6052, a R/W holding circuit 6053, a latch 6054, and a timing generation circuit 6055. The FIFO circuit 6052 functions as an address holding circuit, and responds to a row activation signal supplied from the command buffer 6011 or 6021 through the arbitration logic 6031, thereby storing therein decoded address signals in the order in which they are supplied from the address decoder 6015 or 6025. The row activation signal requests the activation of a row (i.e., word), thereby requesting an access operation. The decoded address signals stored in the FIFO circuit 6052 are supplied to the column decoder 6033 and the word decoder 6035. Moreover, the FIFO circuit 6052 generates a Busy_int.sub.L

signal or a Busy_int.sub.R signal if the core circuit is already in the activated state when access is requested")

Claim 14. A data processor core according to claim 13, said arbitration logic being operable to select one of said at least two buses to route said data access request to, in dependence upon an address location within said at least one memory associated with said data access request. *(Section 0708, lines 1-8 – State the following: "The switches 6061 and 6062 are provided on the input side of the FIFO circuit 6052 and the R/W holding circuit 6053. The switches 6061 and 6062 are controlled by a right/left selection signal supplied from the arbitration logic6031. The switches 6061 and 6062 select signals corresponding to L-port if the left side is chosen, and select signals corresponding to R-port if the right-hand side is chosen")*

Claim 15. A data processor core according to claim 14, wherein said at least two portions of said memory comprise an instruction portion operable to store instructions and at least one data portion operable to store data items, said arbitration logic being operable to route said data access request to one of said at least two buses providing access to said instruction portion when data to be transferred is an instruction and to route said data access request to another of said at least two buses providing access to said at least one data portion when data to be transferred is a data item. *(Section 0519, lines 1-14 – State the following: "Further, the present invention is provided with an operation mode for performing a refresh operation in response to an instruction from the exterior of the device and an operation mode for performing a refresh operation in response to an instruction from the internal refresh circuit. This makes it possible to use the multi-port memory in such a manner that a predetermined external port is assigned as a port for refresh management to receive refresh commands at constant intervals, or to use the multi-port memory in such a manner that the internal refresh circuit initiates refresh operations when all the external ports are in the deactivated state. Accordingly, the present invention*

provides a basis for flexible refresh management that conforms to the system requirements." Section 0187, lines 3-6 – State the following: "The memory array 51 stores therein data that was written and to be read, and includes DRAM memory cells, cell gate transistors, word lines, bit lines, sense amplifiers, column lines, column gates, etc")

Claim 17. A data processor core according to claim 13, wherein said arbitration logic is operable in response to receipt of a data access request from said memory access interface portion and a data access request from said data processing portion, both data access requests requesting access to data in one portion of said at least one memory, to route said data access request from said memory access interface portion to one of said at least two buses providing data access to said one portion of said at least one memory before routing said request from said processing portion to said one of said at least two buses. *(Section 0692, lines 1-5 – State the following: "The arbitration logic 6031 determines the priority of access requests between the port L-port and the port R-port according to the control signals received through the port L-port and the port R-port. For example, access requests are selected and given priority in the order of arrivals to the ports")*

Claim 18. A data processor core according to claim 13, said arbitration logic being operable to detect a wait request from at least one busy portion of said at least one memory, said arbitration logic being operable to not route any data access requests to said busy portion until said wait request is no longer detected. *(Section 0265, lines 1-5 – State the following: "During the Wait period, the master device 200-1 generates a BUSY-A signal or a BUSY-B signal based on the decision made by arbiter 15A. In this example, a BUSY signal is generated with respect to the port that is identified by the arbiter 15A as having received a command earlier")*

Claim 19. A data processing apparatus comprising a data processor core according to claim 1, said data processing apparatus further comprising said at least one

memory. *(Section 0589, lines 4-7 – State the following: "In response to the busy signal /BSYB, a controller such as a CPU connected to the input/output port PORT-B ascertains that the active command ACT supplied to the multi-port memory M is invalid." Section 0600, lines 1-6 – State the following: "FIG. 124 shows a third embodiment of the multi-port memory and the method of controlling the multi-port memory according to the present invention (fifth aspect). The same elements as those of the first embodiment are referred to by the same numerals, and a detailed description thereof will be omitted")*

Claim 20. A data processing apparatus according to claim 19, said data processing apparatus further comprising a direct memory access controller operable to control transfer of data from said external data source to said at least one memory via said memory access interface. *(Section 0601, lines 1-23 – state the following: "In this embodiment, data registers (buffers) 5046a and 5046b that temporarily store respective data signals DQA and DQB between the data latches 5028 and the memory core 5040 are provided in each memory block MB. The data registers 5046a and 5046b operate in association with either one the input/output ports PORT-A and PORT-B. Moreover, the arbitration control circuit 5048 of the arbitration circuit 5034 is different from the arbitration control circuit 5044 of the first embodiment. The arbitration control circuit 5048 does not output the busy signals /BSYA and /BSYB, and no busy buffer is provided in the I/O circuit 5010. Other configurations are almost the same as that of the first embodiment. Namely, in the input/output ports PORT-A and PORT-B, the clock signals CLKA and CLKB, the address signals ADDA and ADDB, the command signals CMDA and CMDB, and the data signals DQA and DQB are transferred through clock terminals, address terminals, command terminals, and data input/output terminals, respectively. The memory block MB includes the DRAM memory core 5040, and further includes control circuitry, decoders, and the like, which are not illustrated.*

Memory cells include capacitors that store electric charge in accordance with values of data signals")

Claim 22. A data processing apparatus according to claim 19, wherein: said at least one memory is divided into at least two portions; and said data processing apparatus further comprising at least two buses, each bus allowing data access to a respective portion of said at least two portions of said at least one memory. *(Section 0459, lines 1-14 – State the following: "According to the present invention, a semiconductor memory device includes a plurality of N external ports, each of which receives commands, a plurality of N buses corresponding to the respective external ports, a plurality of memory blocks connected to the N buses, an address comparison circuit which compares addresses that are to be accessed by the commands input into the N respective external ports, and an arbitration circuit which determines which one or ones of the commands accessing a same memory block are to be executed and which one or ones of the commands accessing the same memory block are to be not executed when the address comparison circuit detects accesses to the same memory block based on the address comparison")*

Claim 24. A data processing apparatus according to claim 22, wherein said at least one memory is a tightly coupled memory. *(Section 0213, lines 1-9 – State the following, which demonstrates the sufficient requirements for a tightly coupled memory: "The transfer gate 122 or 132 opens a predetermined latency after reception of a Read command at a corresponding port in response to the transfer signal supplied from the transfer signal generating circuit 126 or 136. The data of the data latch 121 or 131 is thus transmitted to the data latch 123 or 133, respectively. Thereafter, the data is converted from parallel data to serial data by the parallel serial converter 124 or 134. The data is then transmitted to the output buffer 125 or 135, and is output therefrom")*

Claim 25. A method of transferring data between an external data source and a memory associated with a data processor core, said data processor core comprising a memory access interface portion operable to perform data transfer operations between said external data source and said memory associated with said data processor core and a data processing portion operable to perform data processing operations, said method comprising the steps of: receiving a processor clock signal and a memory access enable signal at the core; performing said data transfer operations through said memory access interface portion clocked by said processor clock signal when said memory access enable signal has a predetermined value, and not performing said data transfer operations when said memory access enable signal does not have said predetermined value; and performing said data processing operations at said data processing portion clocked by said processor clock signal when a processing enable signal has a further predetermined value and not performing said data processing operations when said processing enable signal does not have said further predetermined value. *(Figure 1 – Shows clock input signals) (Section 0697, lines 1-17 – State the following: "In the late-write operation, data and an address provided from the exterior of the device are temporarily stored in buffers, and the data stored in the buffers are written in the memory cells at the next write operation. Namely, the data and address supplied from the exterior of the device at a given write operation are temporarily stored in buffers, and the data stored in the buffers are written during the next write operation in the memory cells specified by the address stored in the buffers. Data and an address newly provided at the second write operation are temporarily stored in the buffers in the like manner, thereby preparing for the following write operation. In this manner, the actual writing of data in memory cells is delayed from a given write operation to the next write operation, thereby making it possible to access the memory core at the start of the next write operation cycle. This*

provides an interface that is compatible to the SRAM interface") (Section 0141, lines 1-4 – State the following: "FIG. 121 shows operations performed when the cycles of the clock signals CLKA and CLKB are the same, and the phase of the clock signal CLKA is ahead of the phase of the clock signal CLKB by more than half a cycle") (Section 0553, lines 6-11 – State the following: "The mode register 5012b, the clock buffer 5024b, the command latch 5026b, the data latch 5028b, the row address buffer 5031b, and the column address latch 5032b corresponding to the input/output port PORT-B operate when an enable signal /ENB supplied from the arbitration circuit 5034 is activated") (Section 0008,lines 1-7 – State the following: "In a multi-port memory having two ports, for example, one SRAM memory cell is provided with two sets of word lines and bit line pairs. One of the ports performs a read/write operation by using one set of a word line and a bit line pair, and the other one of the ports performs a read/write operation by using the other set of a word line and a bit line pair") (Section 0554, lines 1-4 – State the following: "Namely, at the time of activation of the enable signal /ENA, the clock buffer 5024a supplies the clock signal CLKA to a clock terminal CLK of the memory core 5040." Section 0582, lines 9-14 – State the following: "The enable signal/ENA is deactivated in response to the completion of the read operation (FIG. 120-(j)). Here, the precharge operation charges bit lines for transferring data to and from memory cells to a predetermined potential, and deactivates circuitry relevant to row address operations")

Claim 26. A method according to claim 25, said method comprising the further step of generating said data processing enable signal using data processing enable logic present on said data processor core *(Section 0717, lines 1-10 – State the following: "In the Busy logic circuit 6071 corresponding to the left-hand-side port L-port, the OR circuit 6083 put together a plurality of Busy_int signals supplied from the timing generator units 6051*

corresponding to the respective banks, thereby generating a single Busy signal. When the chip-enable signal/CE.sub.L input into the left-hand-side port L-port is asserted (LOW), the Busy signal is output from the NAND circuit 6081 as a negative-logic signal/BuSY.sub.L. The same is applied in the case of the Busy logic circuit 6072 corresponding to the right-hand-side port R-port")

Claim 27. A method according to claim 25, wherein said data processing enable signal is generated in response to detection of a state of said processor clock and a state of said bus in data communication with said read/write port. *(Section 0256, lines 1-9 – State the following: "Differences from the first embodiment shown in FIG. 4 includes the fact that an A port 11A and a B port 12A are provided with BUSY signal I/O units 36 and 46, respectively, and the fact that an address comparator 26 is provided to compare an address of the A port with an address of the B port. If the address comparator 26 detects an address match and thus generates a match signal, an arbiter 15A will switch operation modes of a DRAM core so as to initiate a continuation mode")*

Claim 28. A method according to claim 25, comprising the further step of receiving said data processing enable signal. *(Section 0553, lines 1-11 – State the following: "The mode register 5012a, the clock buffer 5024a, the command latch 5026a, the data latch 5028a, the row address buffer 5031a, and the column address latch 5032a corresponding to the input/output port PORT-A operate when an enable signal /ENA supplied from the arbitration circuit 5034 is activated. The mode register 5012b, the clock buffer 5024b, the command latch 5026b, the data latch 5028b, the row address buffer 5031b, and the column address latch 5032b corresponding to the input/output port PORT-B operate when an enable signal /ENB supplied from the arbitration circuit 5034 is activated")*

Claim 29. A method according to claim 25, wherein said predetermined value and said further predetermined value are the same. *(Section 0560, lines 1-34 –*

State the following: "The address comparison circuit 5042 includes two address matching circuits 5042a and an address comparator 5042b, which detects an order of address arrivals. The address matching circuits 5042a includes a plurality of EOR circuits 5042c, each of which compares corresponding bits of the row address signals RA between the address signal ADDA and the address signal ADDB, and further includes a plurality of nMOS transistors 5042d which correspond to the respective EOR circuit 5042c. The nMOS transistors 5042d each have the gate thereof connected to the output of a corresponding EOR circuit 5042c, the source thereof grounded, and the drain thereof connected with each other. Each EOR circuit 5042c outputs a low level signal when bit values of the row address signals RA match each other between the input/output ports PORT-A and PORT-B, and outputs a high level signal when the bit values of the row address signals RA do not match. The nMOS transistors 5042d are turned off in response to the low level signal from the EOR circuits 5042c, and turns on in response to the high level signal. Namely, match signals /COTN1 and /COIN2 output from the address matching circuits 5042a become floating when all the bits of the row address signals RA match between corresponding bits, and become a low level signal when at least one bit of the row address signals differs between corresponding bits. The two address matching circuits 5042a are arranged at the respective upper end and lower end of the memory block MB shown in FIG. 111 (i.e., arranged close to the input/output circuits 5010). Arrangement of the address matching circuits 5042a close to the I/O circuits 5010 makes it possible to shorten the propagation delay of the address signals ADDA and ADDB all the way to the address matching circuits 5042a. Consequently, the address signals ADDA and ADDB can be compared at an early timing, thereby attaining a high-speed operation")

Claim 30. A method according to claim 25, wherein said external data source comprises a further memory associated with said processor core.

(Abstract, lines 1-5 – State the following: "A semiconductor memory device includes a plurality of N external ports, each of which receives commands, and an internal circuit which performs at least N access operations during a minimum interval of the commands that are input into one of the external ports")

Claim 31. A method according to claim 25, wherein said external data source comprises a further memory, said step of performing said data transfer operations comprising transferring data to and from said further memory via a direct memory access controller. *(Section 0670, lines 1-12 – State the following: "When the same row address signals RA are supplied to the input/output ports PORT-A and PORT-B, a read operation is performed only in response to one of the ports. Because of this, power consumption during the operation can be reduced compared with a case in which respective read operations are performed with respect to both ports. Use of the page buffers 5050a and 5050b eliminates a need for the controller controlling the multi-port memory memory M to detect a busy state of the multi-port memory M even when a page operation is performed. Consequently, the control (in terms of hardware and software) of the controller or the like becomes easier")*

Claim 33. A method according to claim 25, wherein said memory access enable signal comprises a clock signal having a different frequency to said processor clock signal and periodically, at said different frequency, going from a first state having said predetermined value to a second state not having said predetermined value.

Claim 34. A method according to claim 25, comprising a further step of combining said processor clock signal received at said processor clock signal input with said processor clock enable signal using at least one logic gate, and outputting said processor clock signal from said at least one logic gate when said processor enable signal has said further predetermined value and not outputting said processor clock signal when said processor enable

signal does not have said further predetermined value, and receiving said output of said at least one logic gate at said data processing portion such that said data processing operations performed by said data processing portion are clocked by said output of said at least one logic gate. *(Section 0184, lines 1-7 – State the following: "A multi-port memory 10 of FIG. 4 includes an A port 11, a B port 12, a self-refresh circuit 13, a DRAM core 14, an arbiter 15, a refresh-command register 16, a command register A 17, a command register B 18, a refresh-address register 19, an address register A 20, an address register B 21, a write-data register A 22, a write-data register B 23, a transfer gate A 24, and a transfer gate B 25")*

Claim 35. A method according to claim 25, comprising a further step of combining said processor clock signal with said memory access enable signal using at least one logic gate, said at least one logic gate being operable to output said processor clock signal when said memory access enable signal has said predetermined value and not to output said processor clock signal when said memory access enable signal does not have said predetermined value, said memory access interface portion receiving said output of said at least one logic gate such that said data transfer operations performed by said memory access interface are clocked by said output of said at least one logic gate. *(Section 0184, lines 1-7 – State the following: "A multi-port memory 10 of FIG. 4 includes an A port 11, a B port 12, a self-refresh circuit 13, a DRAM core 14, an arbiter 15, a refresh-command register 16, a command register A 17, a command register B 18, a refresh-address register 19, an address register A 20, an address register B 21, a write-data register A 22, a write-data register B 23, a transfer gate A 24, and a transfer gate B 25")*

Claim 36. A method according to claim 25, comprising the further steps of: in response to a data access request requesting access of data in one portion of said at least one memory received from said memory access interface portion and a data access request requesting access to data in a further

portion of said at least one memory received from said data processing portion, routing said data access request to one of at least two buses, said one of said at least two buses providing access to said one portion of said at least one memory, and routing said data access request received from said data processing portion to a further of said at least two buses, said further bus providing access to said further portion of said at least one memory, said routing of said data access requests being performed during the same clock cycle. *(Section 0707, lines 1-12 – State the following: "The R/W holding circuit 6053 responds to a row activation signal by storing therein a Read/Write activation signal supplied through the arbitration logic 6031 from the command buffer 6011 or 6021. The Read/Write activation signal is activated when a Read operation or a Write operation is requested by command signals entered from the exterior of the device. The R/W holding circuit 6053 stores therein an access state (i.e., indicative of a write state or a read state) in response to the Read/Write activation signal. The access state stored in the R/W holding circuit 6053 is supplied to the timing generation circuit 6055 as a signal R/W indicative of an access state") (Sections 0696-0706 – State the following: "The data input output buffer 6013 or 6023 also receives data to be written from the exterior of the device. The data are written in the memory cells selected by a column line among memory cells corresponding to the selected word after traveling through the write amplifier of the data-bus-amplifier-&-write-amplifier unit 6036, the data bus, sense amplifiers, and bit lines. Selection of one of the port L-port and the port R-port at the time of write operation is made by the switch 6037. Further, the data hold buffers 6014 and 6024 are provided for the port L-port and the port R-port, respectively, for the purpose of performing a late-write operation. In the late-write operation, data and an address provided from the exterior of the device are temporarily stored in buffers, and the data stored in the buffers are written in the memory cells at the*

next write operation. Namely, the data and address supplied from the exterior of the device at a given write operation are temporarily stored in buffers, and the data stored in the buffers are written during the next write operation in the memory cells specified by the address stored in the buffers. Data and an address newly provided at the second write operation are temporarily stored in the buffers in the like manner, thereby preparing for the following write operation. In this manner, the actual writing of data in memory cells is delayed from a given write operation to the next write operation, thereby making it possible to access the memory core at the start of the next write operation cycle. This provides an interface that is compatible to the SRAM interface. The refresh timing generation circuit 6040 includes an oscillator 6041 and a divider 6042. The oscillator 6041 generates pulses by oscillation. The generated pulses are subjected to frequency division by the divider 6042, thereby generating a refresh activation signal at constant refresh intervals. The internal address-generation circuit 6039 responds to a refresh activation signal by generating addresses at which refresh operations are to be performed, and supplies these addresses to the address decoder 6015. The refresh activation signal is also supplied to the timing generator 6032. The timing generator 6032 responds to the refresh activation signal by generating timing pulses for performing refresh operations at proper timing, and supplies the timing pulses to the column decoder 6033, the word decoder 6035, etc. In this manner, a refresh command is automatically generated inside the dual-port semiconductor-memory device 6010, thereby making it possible to perform refresh operations at constant intervals with respect to the cell array 6034. Moreover, the dual-port semiconductor memory device 6010 according to the present invention is configured to supply a Busy signal to the exterior of the device if accesses to the same bank are simultaneously made through the port L-port and the port R-port. FIG. 141 is a block diagram showing the

configuration of the timing generator 6032 in relation to the generation of Busy signals. As shown in FIG. 141, the timing generator 6032 includes a plurality of timing generator units 6051 provided separately for respective banks #0 through #n. A bank activation signal generated based on an address input into the port L-port or the port R-port is supplied from the address decoder 6015 or 6025 to one of the timing generator unit 6051 corresponding to the specified bank. If the core circuit is already in the activated state by the timing generator unit 6051 when a bank activation signal arrives, the timing generator unit 51 will generate a Busy_int.sub.L signal or a Busy_int.sub.R signal. The generated Busy_int.sub.L signal or Busy_int.sub.R signal is supplied to the arbitration logic 6031, and is then output to the exterior of the device through the arbitration logic 6031. The timing generator unit 6051 retains the input address, and activates the core circuit immediately after the current operation of the core circuit comes to an end. If a bank activation signal is also supplied from the other port, the input address corresponding to this signal is also retained. In order to first select an address that was retained earlier than the other, the provision of FIFO 6052 or the like is made. When a bank activation signal is supplied to the timing generator unit 6051, the corresponding bank may not be in an activated state. In such a case, the core operation will be started immediately. FIG. 142 is a block diagram showing the detailed configuration of the timing generator unit 6051. The timing generator unit 6051 of FIG. 142 includes a FIFO circuit 6052, a R/W holding circuit 6053, a latch 6054, and a timing generation circuit 6055. The FIFO circuit 6052 functions as an address holding circuit, and responds to a row activation signal supplied from the command buffer 6011 or 6021 through the arbitration logic 6031, thereby storing therein decoded address signals in the order in which they are supplied from the address decoder 6015 or 6025. The row activation signal requests the activation of a row (i.e., word), thereby requesting an access operation.

The decoded address signals stored in the FIFO circuit 6052 are supplied to the column decoder 6033 and the word decoder 6035. Moreover, the FIFO circuit 6052 generates a Busy_int.sub.L signal or a Busy_int.sub.R signal if the core circuit is already in the activated state when access is requested")

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9, 21, and 32 are rejected under 35 U.S.C.103(a) as being unpatentable over Matsuzaki et al. as applied to claims 1, 19, and 25 above, further in view of Jacob (US PGPub 2005/0166033 A1).

Matsuzaki teaches the limitations of claims 1, 19, and 25 for the reasons above.

Matsuzaki's invention differs from the claimed invention in that there is no specific reference to a flash memory being utilized.

Matsuzaki fails to teach claims 9, 21, and 32, which respectively state the following: "A data processor core according to claim 1, wherein said further memory comprises a flash memory operable to store boot up code and said at least one memory comprises an instruction memory, said memory access interface portion being operable to transfer said boot up code from said flash memory to said instruction memory in response to receipt of said processor clock", "A data processing apparatus according to claim 19, said data processing apparatus further comprising a flash memory and an instruction memory", and "A method according to claim 25,

wherein said further memory comprises a flash memory operable to store boot up code and said at least one memory comprises an instruction memory, said step of performing said data transfer operations comprising transferring said boot up code from said flash memory to said instruction memory in response to receipt of said processor clock signal". However, Jacob's invention discloses the following: "A chip level BOOT-SEL (not shown) will have a software window for the boot code running on the k-node through the following auxiliary register access. The initial boot loader residing on the internal ROM can read the state of this pin, and decide the location where the rest of the boot program resides, either present in the, flash memory attached to the integrated circuit or housed in a host processor. For example, if the BOOT_SEL pin is tied low externally, this can indicate the presence of a flash memory connected to the external memory controller with the boot codes programmed in it. Thus, the initial boot loader can jump to the flash memory location and execute the rest of the boot sequence. On the other hand, if this pin is tied high externally, it indicates the absence of the flash memory. Thus, the initial boot loader waits for the host processor to give the k-node the start location of the rest of the boot codes" (Section 0091, lines 1-16). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Multi-Port Memory Based on DRAM Core" of Matsuzaki and Jacob's "System and Method Using Embedded Microprocessor as a Node in an Adaptable Computing Machine" before him at the time the invention was made, to combine the inventions to allow for the utilization of flash memory to include all different types of well-known memory structures of the time, thereby increasing the system's utility.

8. Claims 16 and 23 are rejected under 35 U.S.C.103(a) as being unpatentable over Matsuzaki et al. as applied to claims 1, 13-15, 19, and 22 above, further in view of Tamura et al. (US PGPub 2003/0033573 A1).

Matsuzaki teaches the limitations of claims 1, 13-15, 19, and 22 for the reasons above.

Matsuzaki's invention differs from the claimed invention in that there is no specific reference to a odd or even addresses or where they are stored.

Matsuzaki fails to teach claims 16 and 23, which respectively state the following: "A data processor core according to claim 15, wherein said at least one data portion comprises two data portions, an even data portion operable to store data having an even address and an odd data portion operable to store data having an odd address, said read/write port being operable to transfer data between said processor core and said at least one memory via three buses, a first bus providing access to said instruction portion, a second bus providing access to said odd data portion and a third bus providing access to said even data portion, and said arbitration logic being operable to route a data access request to said first bus when data to be transferred is an instruction, to said second bus when data to be transferred is a data item associated with an odd address and to said third bus when data to be transferred is a data item associated with an even address.", and "A data processing apparatus according to claim 22, wherein said at least one memory is divided into three portions, an instruction portion operable to store instructions, and two data portions, an even data portion operable to store data having an even address and an odd data portion operable to store data having an odd address, said data processing apparatus comprising three buses said read/write port being operable to transfer data between said processor core and said at least one memory via said three buses, a first bus providing access to

said instruction portion, a second bus providing access to said odd data portion and a third bus providing access to said even data portion". However, Tamura's invention discloses the following: "For example, in the flash memory 2 of FIG. 3, the data part PrtD of the sector address SA1 contains even byte data of the sector data 2n (even byte data in each byte data of, for example 512 bytes) EvD (2n), ECC code EvC (n2) as an error detection code relating to even byte data of the sector data 2n, even byte data of the sector data 2n+1 (even 256 byte data in each byte data in each byte data of, for example 512 bytes) EvD (2n+1), and an ECC code EvC (2n+1) as an error detection code relating to even byte data of the sector data 2n+1. The management part PrtM of the sector address SA1 (n) has a good sector code, identification information, other management information and ECC code as management information of the sector address n. The good sector code is a code data representative of whether the sector address SA1 (n) is good or not. The identification code is a code data representative of which of the user data, alternated area, vacant area, or alternate area management area, the corresponding data part belongs to. The other management information may not be particularly defined. The ECC code is error detection and correction redundancy information for good sector code, identification information and other management information. In the flash memory 3 of FIG. 4, the data part PrtD of the sector address SA2 (n) contains odd byte data of the sector data 2n (odd 256 byte data in each byte data of, for example, 512 bytes) OdD (2n), ECC code EvC (2n) as the error detection code relating to odd byte data of the sector data 2n, odd byte data of the sector data 2n+1 (odd 256 byte data in each byte data of, for example, 512 bytes), OdD (2n+1) and ECC code OdC (2n+1) as the error detection code relating to odd byte data of the sector data 2n+1. The management information which the management part PrtM of the

flash memory 3 possesses has meaning which is similar to that of the flash memories of FIG. 3" (Sections 0061-0062). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Multi-Port Memory Based on DRAM Core" of Matsuzaki and Tamura's "Memory Card and Memory Controller" before him at the time the invention was made, to combine the inventions to allow for there to be a portion for odd and even data address storage to enhance system efficiency.

Response to Arguments

9. Applicant's arguments (filed July 13, 2006) with respect to claims 1-32 have been considered but are moot in view of the following ground(s) of rejection.

10. With regards to Claim 1 the Applicant alleges that "Matsuzaki relates to a semiconductor memory device rather than to a data processor core". However, the data processor core in Claim 1 is referenced in the preamble, which does not give it any weight of patentability. Therefore, the Applicant's arguments are moot in view of the prior art.

11. With further regards to Claim 1, the Applicant alleges that "Matsuzaki does not disclose a data processing portion operable to perform further data processing elements. Rather, those operations are performed by a memory core." As stated above however, the fact that the preamble discloses a "data processor core" is irrelevant, and the above art still teaches the rest of the limitations in this section of the claim. The Examiner respectfully points to the underlined portion in the above rejection. Therefore, the Applicant's arguments are moot in view of the prior art.

12. With further regards to Claim 1, the Applicant alleges that Matsuzaki does not disclose a "memory access enable signal". However, the above reference states that the reference address

buffer (a type of memory) operates when the enable signal is activated, so the limitation is, taught by Mastuzaki. Therefore, the Applicant's arguments are moot in view of the prior art.

13. Finally with regards to Claim 1, the Applicant alleges that "there is no disclosure of a data processing portion or a data processing enable signal, let alone the reception by the data processing portion of clock signals only when the enable signal has a certain value." The examiner would like to point out the following: "Since the row address signals RA supplied to the port PORT-B is the same as the row address signals RA supplied to the port PORT-A, the first-arrival signals /FSTA and /FSTB are generated one after another as shown in FIG. 115. The arbitration control circuit 5044 activates the enable signal /ENA and the busy signal/BSYB (FIG. 120-(c) and (d)) in response to the first-arrival signals /FSTA and /FSTB as described in connection with FIG. 119. In this manner, the first one to arrive between the two address signals is determined by using the row address signals RA supplied during the setup time tS and by utilizing a rising edge of the clock signal (CLKA in this example) having an earlier phase. Thereafter, the memory core 5040 corresponding to the row address signals RA operates in response to the activation of the enable signal /ENA (FIG. 120(e))" (Section 0579). It is important to note that the CLKA signal is being utilized above, while the CLKB signal is not. Therefore, the prior art does in fact teach the limitations of the claim. Therefore, the Applicant's arguments are moot in view of the prior art.

14. Claims 2-36 remain rejected due to either their dependence on Claim 1, or due to their lack of argumentative support.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-Th, from 8-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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